

### **REMARKS**

Claims 43-48, 51-67 and 70-88 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

### **REJECTION UNDER 35 U.S.C. § 103**

Claims 43-48, 51-57, 59-67, 70-76 and 78-80 stand rejected under 35 U.S.C. §102(b) as being unpatentable over a dissertation by Oh entitled "Analog CMOS Implementation of Artificial Neural Networks for Temporal Signal Learning" (Oh) in view of article by Lehmann et al entitled "MixedAnalog/Digital Matrix-Vector Multiplier for Neural Network Synapses" (Lehmann). This rejection is respectfully traversed.

Oh relates generally to an analog implementation of an artificial neural network. As conceded by the Examiner, Oh does not teach a learning circuit that updates a local weight and stores the local weight in a capacitor as well as in a digital memory within the cell. The Examiner relies upon Lehmann to teach this aspect of the present invention.

Lehmann relates generally to a mixed matrix-vector multiplier for neural networks. Of note, Lehmann suggests the use of a capacitor as an "analog extension" to a digital memory. This means that the analog capacitor will accumulate the difference between what the digital memory is storing and what a learning method may need the value to be (i.e., it computes a differential and then uses a counter to increment the digital memory). Such an "analog extension" has no operability support or justification. There is no supportive engineering analysis that ensures this method

would work and it is highly likely that it will face serious stability issues. Lehmann further assumes that a learning method would be able to do that without any considerations that the learning method will encounter instability. It is noteworthy that Lehmann does not provide any specific teachings for how learning would be implemented but merely outlines an approach. Thus, how learning is implemented in hardware is in fact speculative and open to questions including instability. Thus, this combination of references does not yield a predictable result. *KSR International Co. v. Teleflex Inc.* 82 USPQ2d 1385 (2007). In addition, the proposed modification by the Examiner cannot render the teachings of Oh unsatisfactory for its intended purpose nor can it change the principle of operation. See, MPEP 2143.01. For these reasons, applicant contends that the teachings of Lehmann cannot be combined with Oh.

Furthermore, the use of a capacitor as an “analog extension” means that the capacitor in Lehmann is in the same path or in series with the digital memory, thereby creating a mixed-mode arrangement. In contrast, applicant’s invention discloses a cell arrangement where a capacitor is arranged in parallel with a digital memory. In this way, applicant’s invention implements learning methods entirely in an analog domain, thereby avoiding the mixed mode issues (i.e., non-convergence) associated with Lehmann. Pending claims have been amended to clarify this aspect of the present invention. Basis for this amendment may be found throughout the application as originally filed, including Figure 2. For this additional reason, the pending claims define patentably subject matter over the relied upon combination of references. Accordingly, Applicants respectfully request the Examiner reconsider and withdraw these rejections.

## CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested.

If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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